XILINX

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An Architecture to Stamp Asynchronously the TOD with 1 ps Resolution

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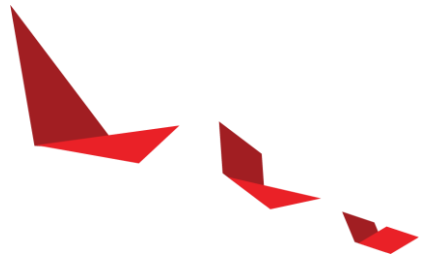
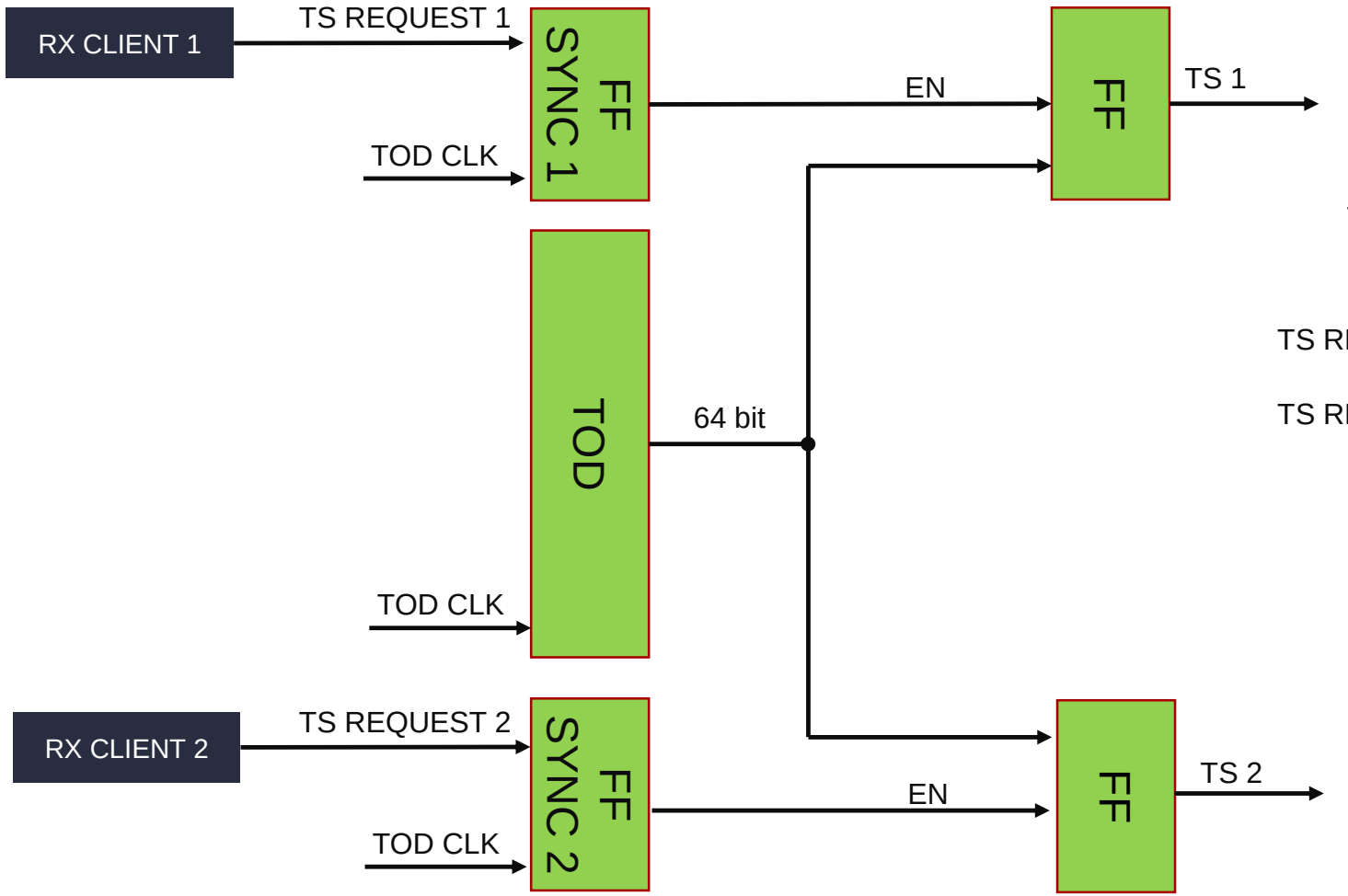
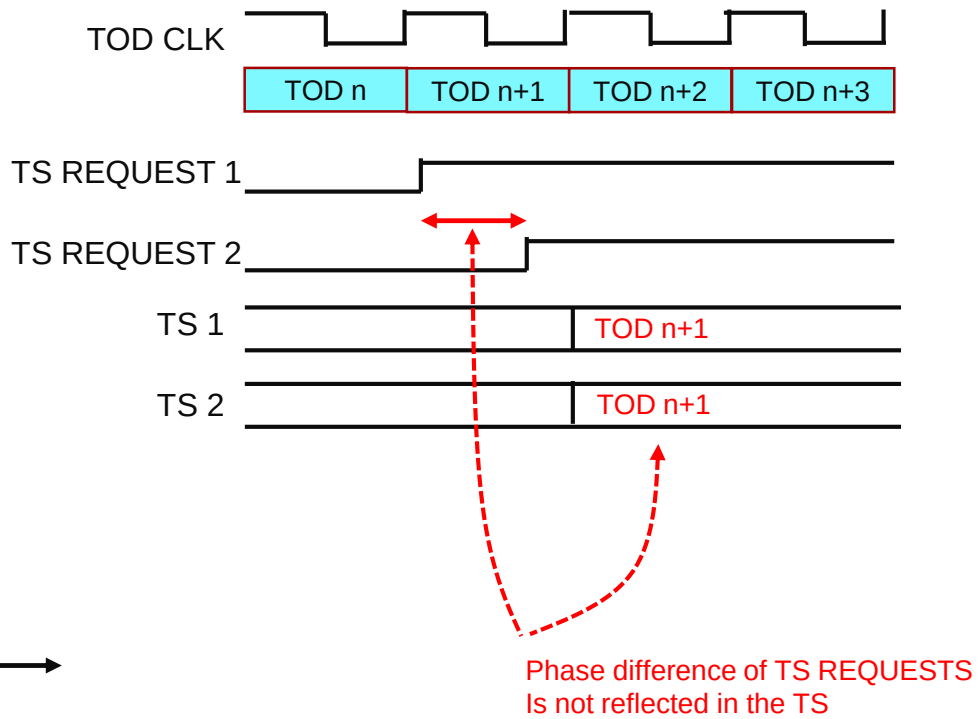


- Introduction
- The problem of stamping the TOD
- Architecture
  - Comparison with classical methods
  - Advantages
- Conclusion

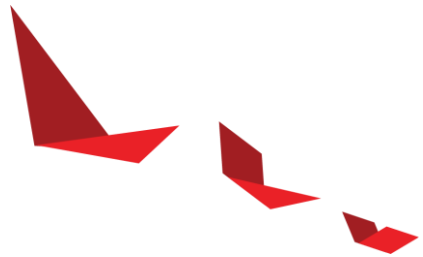
The Problem: Stamping the TOD





TOD sampling error: TS 1 and TS 2 are equal, althogh there is a phase difference between TS REQUEST 1 and 2

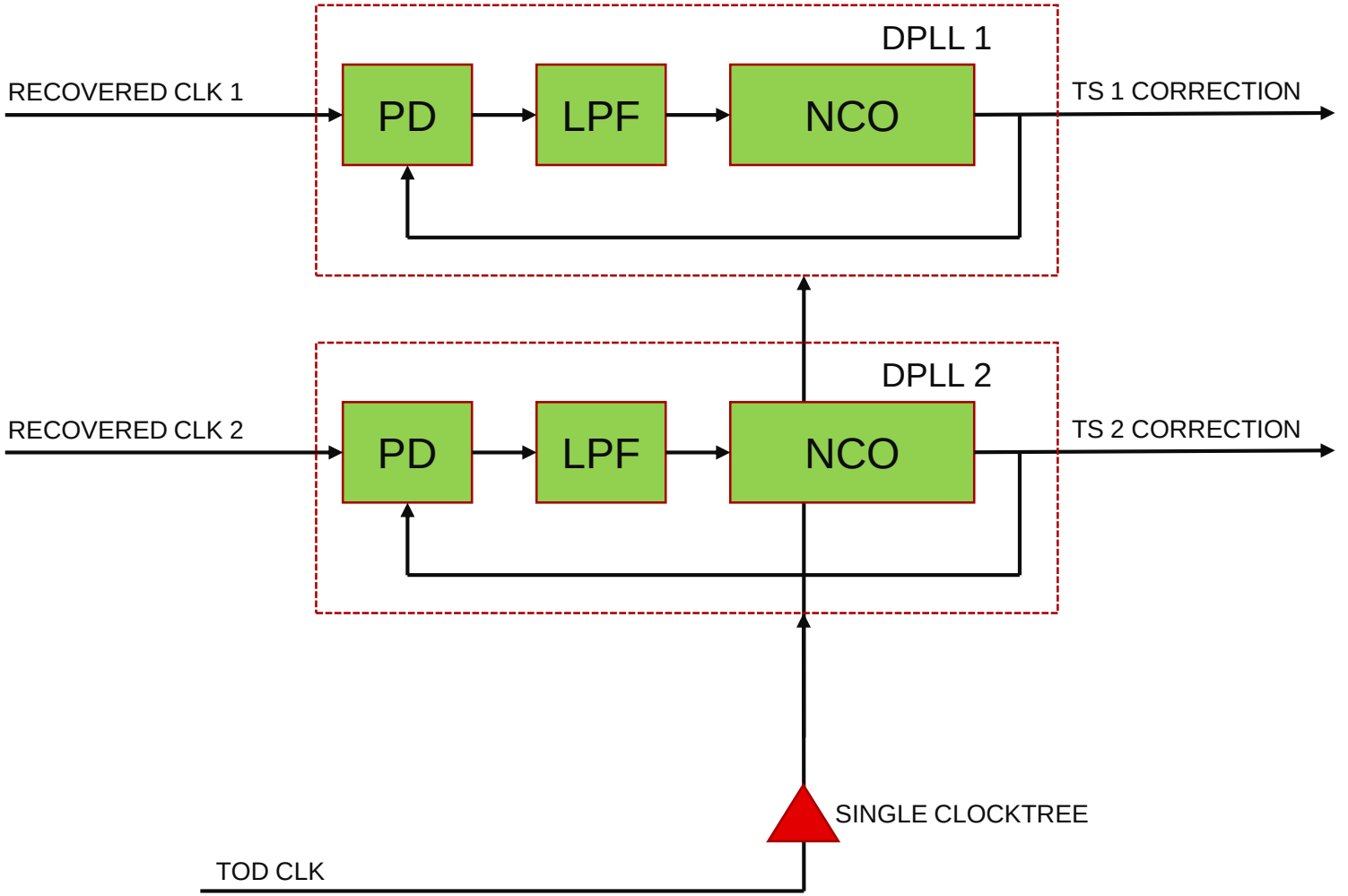
Classical Solutions



- Increasing the TOD clock frequency
- Generating a polyphase TOD.

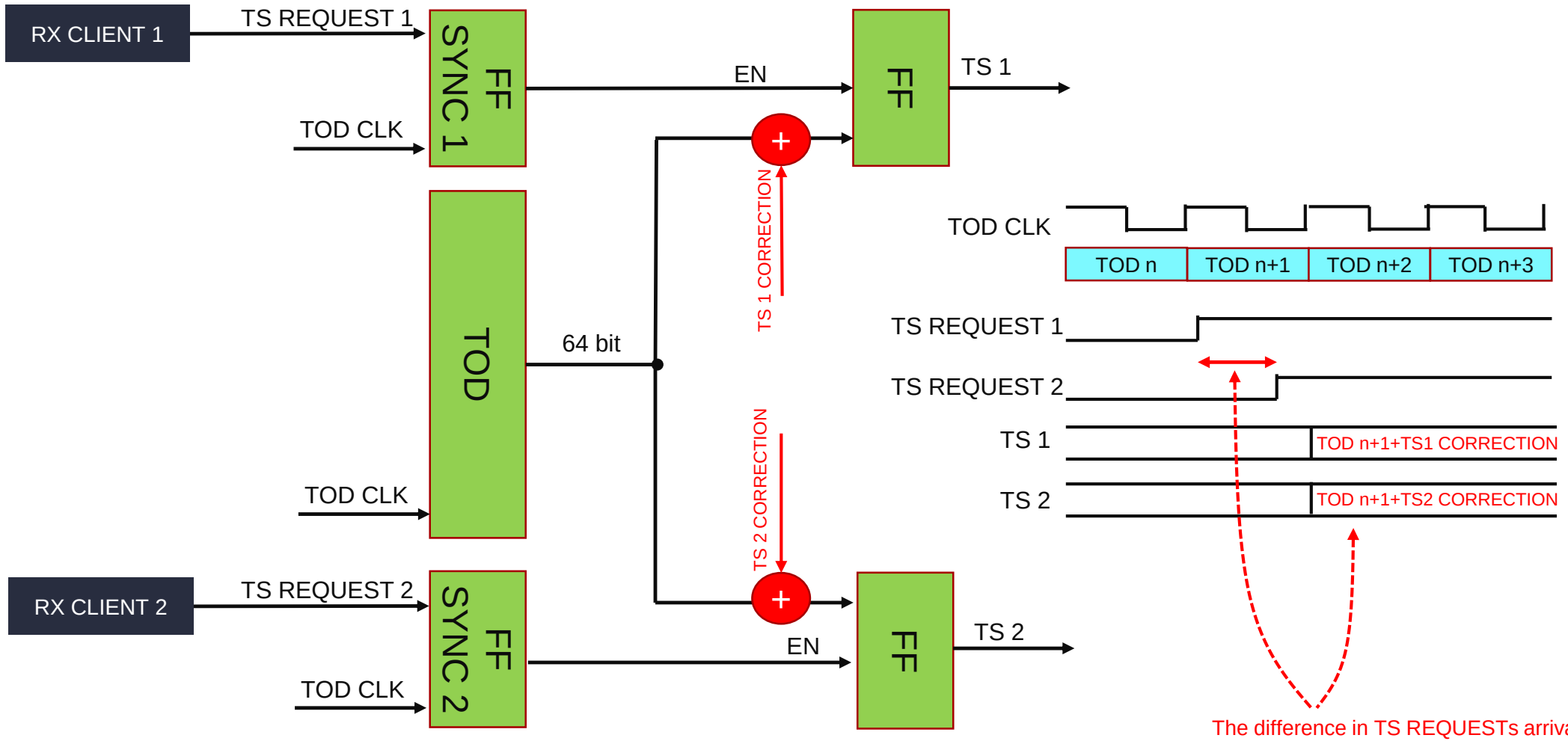
Improvement is Limited by Silicon Technology

Architectural Improvement

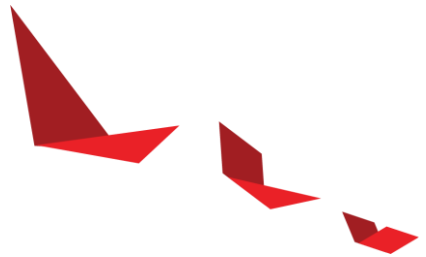


Improvement Is Limited by Architecture, not by Silicon

Accurate TOD Stamping: Architecture



Conclusions



- The electronics plays a role in the accuracy of the overall TOD distribution
- In ITSF 2019, I focused on techniques to mitigate the effect of latency change in transceivers.
- This year, I focused on architectures to mitigate inaccuracies in asynchronous TOD stamping.
  - Paradigm shift: focus on architecture vs focus on silicon technology
- Accuracy is limited by architecture, rather than technology.